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Abstract

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Design Considerations and FPGA Implementation of a Wideband All-Digital Transmit Beamformer with 50% Fractional Bandwidth

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***Abstract*— In this work, we report design and implementation of an all-digital transmit phased array. The key design considerations have been reviewed including applications of multi-core DSM and wideband beamformer based on space-time theory. The built prototype of 8-element array using a commerical FPGA board demonstrated the feasibility of designing real-time wideband digital beamformer. The measured beam pattern for RF frequency of 2.5 GHz with 1.25 GHz bandwidth agreed well with simulation. To the authors' knowledge, this fractional bandwidth of 50% is the widest one reported so far. This advances the state-of-the art in terms of fractional bandwidth by more than 40 times, which shows that all-digital transmitter is a very promising technology for next generation directional communications such as 5G and beyond.**

***Keywords*— all digital transmitters, digital wideband beamformers, massive phased arrays**

I. Introduction

Phased array covering wide bandwidth is highly desirable yet technical challenging. Conventional beamforming techniques employed analog phase shifters where the signals feeding the antenna are progressively phase shifted so as to form a beam in the far-field. In contrast, digital beamformers can offer higher flexibility in providing electronically steerable beams[1], [2]. Notwithstanding, as we move into 5G and beyond, digital beamforming is facing cost and complexity challenges for fully connected array, where dedicated RF path is required for each antenna element. The scaling of such digital arrays thus becomes prohibitive.

With significant advancements of field programmable gate arrays (FPGA), moving the phased array design to digital domain is a viable solution and key topic to explore. There has been few prior work reported on implementing these all digital array architectures at transmit side on the basis all digital transmitters (ADTs) [3], [4]. An all digital phased array comprising 8-elements is reported in [5], which is the state of the art. However, this provides only 25 MHz of signal bandwidth. The wideband implementation of ADT array is very attractive but facing significant design challenges. So far, wideband digital beamformers are based on either true-time delay, fractional FIR filters or FFT [6], [7]. They are stable and provide reasonable linear response but digitally very expensive. Hence, novel architecture of all-digital phased array with reduced complexity is strongly needed.

To this end, our work here reports a recent development of an all digital beamformer/phased array that comprises two novel enabling architectures 1) all digital transmitter, and 2) wideband beamformer based on 2D-space time filter network theory. The key design considerations, prototype development, and experiment results are introduced in the following sections. Our measurement results demonstrated the widest fractional bandwidth of an all-digital array of 50% implemented in a commercial FPGA.

II. Design Considerations

A. All Digital Transmitter

In an radio-frequency (RF) transmitter, it is known that mixers and DACs contribute the most towards the size, weight and power (SWaP) values. The mixers implemented in analog domain are bulky and tend to become expensive as the array size increases, whereas the DACs provide a better bit resolution at a cost of increased power consumption. One of the key advantage of the ADTs is to relax the DACs requirement and also to perform a digital up-conversion with high flexibility. Fig. 1 shows the block diagram of an ADT that has been proposed in [4].

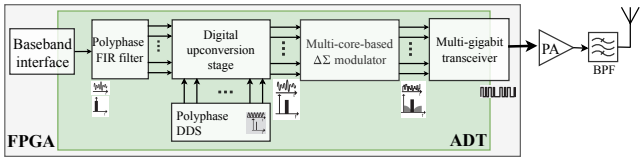

Fig. 1. Block diagram of an all digital transmitter (ADT).

The baseband data stored in FPGA memory is divided into several phases using a polyphase FIR filter to achieve higher sampling rates dictated by the serializers on the FPGA. The polyphase digital upconversion (DUC) stage receives the baseband signal and applies a mixing operation with a polyphase Digital Direct Synthesis (DDS) acting as a local oscillator (LO). The resultant signal is forwarded to the multi-core delta-sigma (DSM) module.

Multi-core DSM module performs the pulse-encoding techniques based on $\Delta - \Sigma$ theory so as to remove the in-band quantization noise of the 1-bit pulses to be transmitted by the multi-gigabit transceivers (MGTs). It contains parallel delta-sigma modulators to process the polyphase signals and is based on propagation of state registers [8]. It consists of three modules 1) deinterleaver 2) parallel DSM modulator, and 3) interleaver. The principle of operation is to rearrange and combine the data from different phase paths (performed by deinterleaver), transmit it to the parallel DSM modulator, and finally rearranging and combining back to the polyphase paths (performed by interleaver). Each core of the multi-core DSM

modulator contains a generic error-feedback DSM architecture as shown in Fig. 2. Such a filter transfer function is given by,

$$Y(z) = STF(z)X(z) - NTF(z)E_q(z), \tag{1}$$

where, $STF(z)$ is the Signal transfer function, and $NTF(z) = 1 + H(z)$ is the noise transfer function with $H(z)$ as the feed-back loop transfer function. Here, the quantization noise is modeled by a random noise signal $NTF(z)$, and can be either an FIR or an IIR filter. The filter $H(z)$ is realized to provide nulls for the NTF in the desired band. Extensive details are omitted here and can be found in [8].

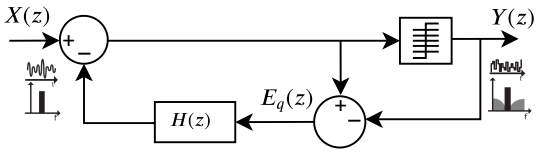

Fig. 2. Architecture of an error-feedback DSM modulator.

The output data from the multi core DSM module is serialized and converted to high-speed digital pulses through MGTs. These pulses are amplified and finally subjected to bandpass filtering stage to reconstruct the RF analog waveform before being radiated by the antennas. This RF-ADT design is one of the key basis of the current work.

B. Wideband Beamformers based on Space-Time Networks

Digital beamformers that are based on 2D space-time theory serve better for wideband applications. Also known as network resonant digital plane wave filter (NR-DPWs), these were proposed by Bruton and Bartley in 1985 [9] and have been used widely in receive mode. It was also experimentally verified in one of the author's work[10]. Recently we made a proposal [11] on their applicability in the transmit mode as well. The wideband nature comes from their time-domain approach. These filters are IIR based and are designed using resistively terminated passive low-pass LC-ladder circuit prototypes such as the one shown in Fig. 3(a). The network resembles the conventional 1D filter topology corresponding to temporal frequency domain $s_{ct} = j\omega_{ct}$, but extended to another dimension i.e., spatial dimension $s_x = j\omega_x$. The 2D-magnitude response $|H(s_x, s_{ct})|$ of such a circuit is given by,

$$H(s_x, s_{ct}) = \frac{Y(s_x, s_{ct})}{X(s_x, s_{ct})} = \frac{R}{R + L_x s_x + L_{ct} s_{ct}} \tag{2}$$

By choosing $L_x = \cos\theta$ and $L_{ct} = \sin\theta$ and certain value of R in Eq. (2), the 2D magnitude response is plotted and shown in Fig. 3(b). In the magnitude response, the region where the magnitude is non-zero i.e., region of support (ROS) lies on a straight line oriented at an angle θ to the ω_{ct} axis. With reference to [9], for an N-element uniform linear array (ULA), a beam pointing at angle ψ from the array broadside is related to angle θ (in the plot) by the relation $\tan\theta = \sin\psi$. Thus by configuring the filter parameters, a beamformer can be implemented to selectively enhance or transmit the desired signal at angle ψ for the entire temporal bandwidth. The

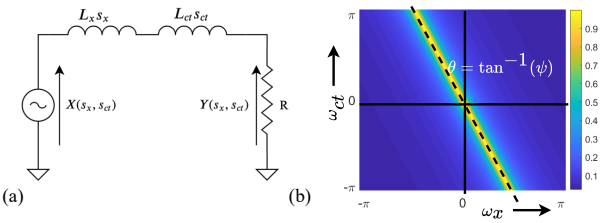

Fig. 3. (a) Prototype network of 2D network resonant digital plane-wave filter and (b) 2D magnitude response of filter $|H(s_x, s_{ct})|$.

difference equation can be found by applying 2D bilinear transform $s_k = (1 - z_k^{-1})/(1 + z_k^{-1})$, $k \in (x, ct)$ to Eq. (2), and followed by applying inverse z-transform under zero initial conditions. Assuming $x(n_x, n_{ct})$ and $y(n_x, n_{ct})$ to be input and output to the filter respectively, the simplified difference equation is given by,

$$\begin{aligned} y(n_x, n_{ct}) &= \sum_{p=0}^{1}\sum_{q=0}^{1} x(n_x - p, n_{ct} - q) \\ &\quad - \sum_{p=0}^{1}\sum_{q=0}^{1} b_{pq} y(n_x - p, n_{ct} - q); \quad p + q \neq 0 \\ \text{where} \quad b_{pq} &= \frac{R + (-1)^p L_x + (-1)^q L_{ct}}{R + L_x + L_{ct}} \end{aligned} \tag{3}$$

Direct-form I realization of such a filter in transmit mode is shown in [11]. Since the filter is recursive and implemented as a systolic array (parallel processing array of identical modules), it only needs its first module to be excited. This greatly reduces digital complexity since majority of the multipliers can be omitted.

III. Architecture of All Digital Phased Array

By taking into account the key design considerations in the previous section, the architecture of the proposed All Digital Phased Array is shown in Fig. 4. The details are as follows:

A. Multi-Core 2D NR-DPW Filter

To develop the proposed architecture from the ADT, the NR-DPW beamfilter design has to be integrated to it. However, the challenging part is that the beamfilter architecture was defined only for a single core which cannot run beyond 300 MHz (limited by FPGA baseband clock), and to achieve higher sampling rates as dictated by MGTs, a polyphase implementation is needed. Hence a multi-core 2D NR-DPW beamfilter based on propagation of state registers is designed for this work. Each core of the multi-core beamfilter contains a direct-form I realization of the difference equation defined in Eq. (3). The temporal upconverted baseband samples from polyphases are connected to the corresponding cores of the first module in the filter design. Since the beamfilter is recursive and implemented as a systolic array, outputs from each core of a module are passed to the respective core of the next module. Beamformed outputs from each module are then passed to the corresponding multi-core DSM modulator. It has to be mentioned that due to the filter architecture we only need one

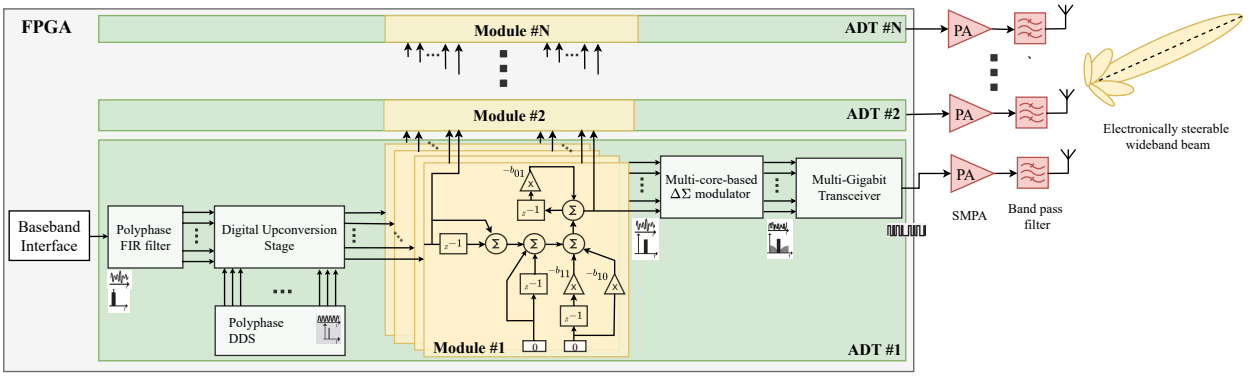

Fig. 4. Proposed architecture for the All Digital Phased Array.

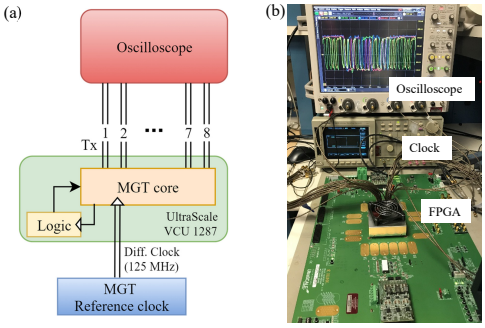

Fig. 5. (a) Verification setup block diagram and (b) experimental setup.

digital upconversion stage for the N-element array leading to greater reduction in hardware resources.

B. Multi-Core DSM Modulator

A multi-core DSM modulator based on error-feedback bandpass $\Delta - \Sigma$ modulator is employed for this work. An IIR filter is selected to model the $NTF(z)$, since the FIR filter with two quantization levels leads to unstable realization. To accommodate the targeted wide bandwidth of 1.25 GHz, a 3 notch IIR filter is designed whose $NTF(z)$ is given by [8],

$$NTF(z) = \prod_{i=1}^{3} \frac{1 + \alpha_i z^{-1} + z^{-2}}{1 + r\alpha_i z^{-1} + r^2 z^{-2}} \ , \tag{4}$$

where $\alpha_i = -2\cos(2\pi F_i/Fs)$, with F_i as notch frequencies and F_s as modulator sampling frequency. Notch frequencies are selected such that the operational bandwidth is 1.25 GHz with a center frequency at 2.5 GHz with r = 0.75 (trade-off between the bandwidth and the stability of the filter). Sampling frequency is chosen to be 10 GSps to maintain an oversampling factor of 4. The feedback loop transfer function $H(z)$ can be computed from Eq. (1) and Eq. (4) and is given by,

$$H(z) = \left(\sum_{i=1}^{6} a_i z^{-i}\right) \Big/ \left(1 + \sum_{i=1}^{6} b_i z^{-i}\right) \tag{5}$$

where the coefficients a_i and b_i can be computed using the reference [8]. Thus, the multi-core second order bandpass DSM modulator is designed using the IIR feedback loop transfer function $H(z)$ shown in Eq. (5). Following the pulse encoding process, the parallel stream of binary high speed pulses are serialized by the MGTs and interfaced to the analog front-end.

IV. Hardware Implementation

For proof-of-concept verification, All Digital Phased Array of 8-elements at 2.5 GHz supporting 1.25 GHz bandwidth (corresponding to 50% fractional bandwidth) is implemented. To validate the proposed design, a Xilinx ZUC1287 evaluation board featuring XCVU095 FPGA is selected. The digital design clocking at 250 MHz with 40 phases is implemented in the FPGA. The 2-level output from the 40 phases from 8 channels are serialized through MGTs that are configured to 10 GSps. Due to unavailability of anechoic chamber, the proposed work is verified offline using an oscilloscope. The setup block diagram and the experimental setup for verification of the proposed work is shown in Fig. 5. Quads Q228 and Q229 in the MGT core are utilized to transmit the signals out that are received by a 4-port real time oscilloscope (Keysight DSA-X 92504Q). Tektronix AWG610 provides the 125 MHz FPGA differential reference clock. Due to challenges of measuring all 8-channels at once, one channel is used as reference to provide the synchronization between the channels. Calibration of all the channels is achieved by transmitting a preknown data and correcting for phase mismatches.

V. Performance Evaluation

A 16 QAM test signal spanning a 1.25 GHz bandwidth is created and stored in FPGA memory that is upconverted and passed to the beamformer with filter coefficients set to point the beam towards $\psi = 30°$. The beamformed signals from all the channels is captured in the scope memory and signal analysis is performed in Matlab. The simulation and measurement results are shown in Fig. 6. The simulation are the values obtained from the fixed point design captured in Matlab Simulink. Both the results indicated the beams contain their ROS aligned at $\psi = 30°$ along the desired bandwidth of 1.25 GHz centering at 2.5 GHz (yellow region). The quantization noise is moved to out of the band (green region) and the levels in measured and simulations were reported to be -28 and -29 dB respectively.

The beam performance of the implementation was evaluated by plotting the beampattern. To plot the beampattern

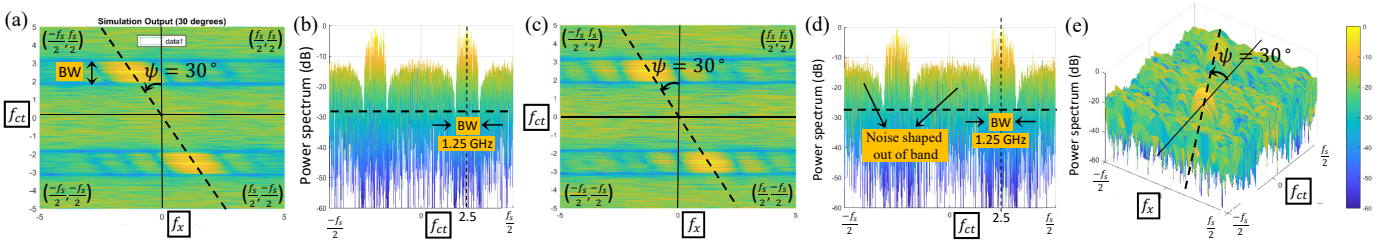

Fig. 6. Comparison of measured and simulated 2-D spectra for the 8-element all digital phased array for $\psi = 30°$. Simulated results for (f_x vs f_{ct}) and (Gain vs f_{ct}) in (a) and (b) respectively; Measured results for (f_x vs f_{ct}) and (Gain vs f_{ct}) in (c) and (d) respectively; 3D view for the measured response is shown in (e). In figure f_x = spatial frequency, f_{ct} = temporal frequency and f_s is the sampling frequency (f_s =10 GHz).

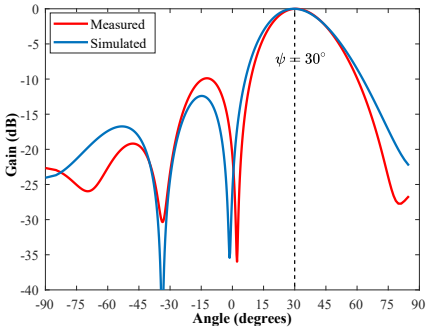

Fig. 7. Comparison of simulated and measured beam pattern at 2.5 GHz.

the quantization noise needs to removed first, so a bandpass filter is implemented in matlab for the required band. The comparison of simulated and measured beampatterns for $f = 2.5$ GHz is shown in Fig. 7. The measured and simulated results are reported in the Table 1.

Results indicate a good agreement between the simulation and measurements. The degradation in side lobe level is assumed to occur due to measurement imperfections.

Table 1. Comparison Between Simulated and Measured Beam Patterns.

Parameter	Measured	Simulated
ψ(degrees)	30	30
Side-lobe level	-10	-12.5

Table 2. Resource Utilization of Proposed Design.

Resource	Utilization	Available	%
LUT	215609	537600	**40.1**
LUTRAM	39924	76800	**52**
FF	126053	1075200	**11.7**
GT	8	64	12.6
BUFG	3	960	0.3

The design captured in Matlab Simulink is ported to Vivado to find the timing and resource allocation from the implemented netlist. The timing reports resulted in 252.5 MHz. The other figures of merit are mentioned in the Table 2. Comparing to the FPGA resource allocation for the RF ADT implementation in [4] that covered 75 % of its LUT memory usage, the proposed design manages to do it with only 52 % leading to greater resource efficiency.

The proposed work is verified at 2.5 GHz, however it can be scaled to sub 6 GHz and 28 GHz 5G applications. The commercial FPGAs containing serializers (GTYs) that can go upto 28 GSps, can be used for realizing sub 6-GHz ADTs with an oversampling factor of 4. Sub-7 GHz implementations when employed with an external analog mixer can realize a 28 GHz ADT. And also since the proposed work is naturally scalable, it can achieve high gains.

VI. Conclusion

For the first time, we designed and reported the implementation of an ultra wideband all-digital transmit beamformer with 50% fractional bandwidth. Key features of the design including significantly reduced digital resource and real-time computation complexity has been demonstrated using commercial FPGA. Digitization of phased array towards an all-digital beamformer manifests itself as a key enabler for next generation mobile communications.

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