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Abstract

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CDM-based 4-Channel Digital Beamforming Transmitter Using a Single DAC

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***Abstract*—In recent years, digital beamforming (DBF) is gaining more attention for directional communication systems, thanks to its flexibility for beamstearing over both analog- and hybrid-beamforming systems. However, conventional digital beamforming requires the use of independent Digital to Analog converters (DAC) and RF chain for each antenna element, which poses significant challenges such as cost, power consumption and heat dissipation. In this work, we present for the first time a novel low-cost solution with reduced hardware for DBF. Digital beamformed multiple baseband signal channels for different antenna elements through a single DAC by using digital signal processing. We implemented coding schemes in digital domain and successfully decoded and recovered them in the analog domain. The measured recovered signals before its fed to antenna elements for the performance evaluation of the system was done via real-time scope. The demonstrated technique provides cost-effectiveness and reduction in size of the array system while keeping the integrity of the signals, required for the next-generation wireless communication systems.**

***Index Terms*—Digital beamforming, FPGA, CDMA multiplexing, antenna array, beamforming hardware, DSP.**

I. Introduction

Beamforming antenna arrays have been reported for a long time in history and have regained popularity in wireless communication systems with 5G [1] [2] [3]. However, with the growing popularity and demand for applying beamforming to the most commonly used telecommunication systems, it becomes very crucial to make such systems affordable. Thus enabling their wide acceptance, particularly for cost-sensitive applications such as mobile communications and WiFi networks. In contrast, to attain outstanding performance, we often sacrifice on the cost and size of the set-up. Moreover, power consumption and heat dissipation add to the restraints that are posed by the traditional beamforming set-up. Conventional digital beamforming architecture performs signal processing (weighting factor and phase change) in the digital domain before conversion to analog by DAC [4]. These analog signals are upconverted and fed to antenna elements of the antenna array to achieve beamforming. In these systems, major part of signal processing is done in the digital domain. Consequently, providing more control and enabling users to create much more complex beam patterns. Such flexibility and control are particularly required to support multi-user MIMO system, where simultaneous and multiple beam streams in a wide variety of angles are necessary.

However, traditional digital beamforming systems offer more flexibility, but the large number of DACs and associated circuitry inevitably add to the challenge in its implementation. The large number of DACs increases power consumption, heat and the overall system cost. For example; if an antenna array has N-antenna elements, then we would require N-DACs to set-up a digital beamforming system. As mentioned earlier, this prohibits the cost-effective and heat manageable DBF solution owing to large RF components and Data converters, in-spite of its flexibility. Recently, digital signal processing and RF path sharing have gained popularity to design more efficient and complex systems with possibilities for cost optimization [5]–[8]. In this paper, we present and propose a new technique to expand digital beamforming for a transmitter system that enables beamforming with significantly less number of DAC's.

In the CDMA-Based Digital Beamforming transmitter architecture as shown in figure 1, we retained all the traditional parts that allow us to create beamforming streams for multiple antenna elements. However, instead of feeding them to DAC's we multiplex them to a combined stream which allows us to reduce the number of DAC required dramatically. We used the CDMA scheme in the digital domain to multiplex signals and converted them to analog signals using a single DAC. We recovered the corresponding analog signals by multiplying them in the analog domain using synchronized digital code signals. These signals are filtered through a narrow band filter and then fed to antenna elements to enable beamforming.

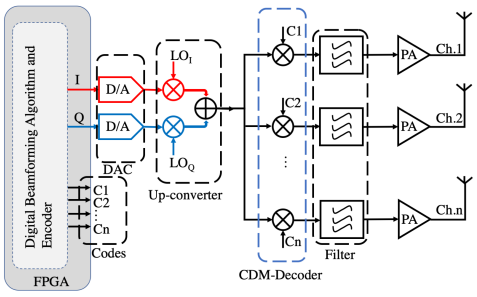

Fig. 1. Architecture of proposed digital beamforming transmitter system.

A drastic reduction in the required number of DAC's in

CDM beamformer results in an overall reduction of cost, power consumption as well as the heat generated by the system. Note that the proposed concept is fully scalable to support a higher number of antenna elements for adjustable beam steering and can also be used for a wide range of RF frequencies. In this paper, we used a specific case of 4-channel digital beamforming transmitter using a single DAC to demonstrate the feasibility of such system.

The rest of this paper is organized as follows: In Section 2, we discuss the system architecture, design and implementation details. In Section 3, we describe the experimental setup and present the results from the implemented system. Also explaining, the post-processing done and demonstrate beam-forming performance. In section 4, we conclude the results and contributions.

II. System Overview and Implementation

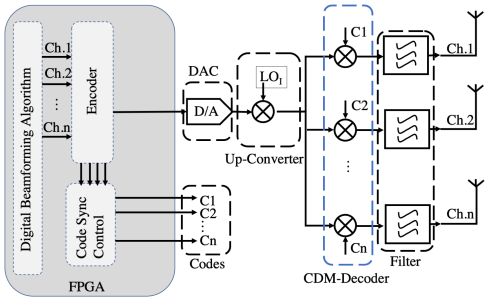

Fig. 2. Implemented CDM-digital beamforming transmitter system.

In a CDM based beamformer transmitter system, we process the multiple beamforming streams digitally in FPGA. As shown in figure 2 we add an encoder to the conventional Digital beamforming transmitter that implements the code generator in FPGA. The encoder generates the codes and multiplies them with different digital streams to combine them into a single digital stream. The copy of these codes is also produced through the digital I/O pins of FPGA, these code signals are needed for the recovery of the analog signal in the RF domain.

For our implemented system we designed the system to have the ability to use the baseband signal stream of up to 15MHz and support 4 elements antenna array.

TABLE I
Design specifications for the CDM based DBF transmitter.

Parameter name	Value
Base band signal rate	x Hz (given)
Base band digital signal resolution	R bit (given)
Number of channels to multiplex	n (given)
Code rate	$>= n.x$ Hz
Code resolution	$>= n$ bit
DAC rate	$>= 2.n.x$ Hz
DAC resolution	$>= R$ bit

We used the Xilinx Virtex 7-series FPGA development board to implement the digital parts of the system. This board features high-speed digital elements and interfaces that facilitate us to implement the design onto the board. We used the FMC connector on the development board to interface the

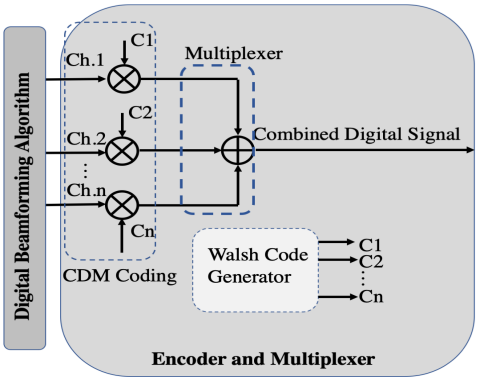

Fig. 3. Encoder implementation in FPGA.

Code Index	Bit-0	Bit-1	Bit-2	Bit-3	Bit-4	Bit-5	Bit-6	Bit-7
0	1	1	1	1	1	1	1	1
1	1	1	1	1	-1	-1	-1	-1
2	1	1	-1	-1	-1	-1	1	1
3	1	1	-1	-1	1	1	-1	-1
4	1	-1	-1	1	1	-1	-1	1
5	1	-1	-1	1	-1	1	1	-1
6	1	-1	1	-1	-1	1	-1	1
7	1	-1	1	-1	1	-1	1	-1

Fig. 4. 8-Bit Walsh code table.

high-speed DAC which allowed us to test our system with a variety of frequency bands efficiently. However, another development board with lower specifications can be used as long as it meets the implementation requirements of different sections as per table I. Different sections of the system as well as their implementation are as follows:

1) Encoding: Encoding in CDM beamforming transmitter is done using Walsh codes with requirements as per the Table:I. Walsh codes are orthogonal by nature and ensure reliable recovery for beamforming. The encoding and code generation parts are implemented in the digital processing hardware by FPGA. Codes are generated by using linear shift registers on FPGA. These rotating shift registers are synchronous to the stream data to enable efficient coding. The code length and code rate are expressed as a function of the number of channels to be multiplexed and the rate of the signal stream as follows. For a given stream signal rate xHz and the number of channels to be multiplexed n,

$$code\_length >= nbits \quad (1)$$

$$code\_rate >= n.xHz. \quad (2)$$

For our system of 4 channel streams with a bandwidth of 15MHz each, we require the minimum code length of 4-bits and the code rate to be greater than $(4 * 15)MHz$. For the implemented design on FPGA as shown in the figure 3, we have used 8 bit Walsh codes. Thus giving us the ability to test the effects of different code properties on the beamforming results. The index diagram of 8-bit Walsh codes is shown in figure 4. Since we used 8-bit codes, the code rate used was $(8 * 15)MHz$. The codes used for the 4-channel implementation are the code index 1,3,4 and 7. Codes of index 1 and 7 have different frequencies and are orthogonal, while Codes of index 3 and 4 have the same frequency and are orthogonal.

2) Multiplexing: The encoder passes coded signal streams to the adder where it adds up all the encoded signals to create a single stream. The adder blocks are implemented to be synchronous with the code rate for addition without any loss

of information. This process generates the stream of data at $(n.x)Hz$. This stream is then sent to a DAC. For implemented design we used the multiplexing adder rate of $(8 * 15)MHz$ using the code rate Eq(2).

3) Digital to Analog Conversion: Digital to analog converter(DAC) converts the digital signal stream to a baseband analog signal. By calculating the spread of codes and their spreading effect, the required DAC rate and DAC resolution can be calculated. DAC rate and DAC resolution is given as a function of the code rate and stream data resolution as follows:

$$DAC_{rate} >= code\_rate Hz \tag{3}$$

$$DAC_{resolution} >= Rbits, \tag{4}$$

where $code\_rate$ can be derived from equation2 and R is the resolution of the digital baseband signal. We designed the entire digital system in the MATLAB system generator, simulated its performance, and then implemented it.

4) Frequency Up conversion: As shown in the Fig. 1, using the resulting analog baseband signal generated by the DAC, we up-convert the signal to RF signal. The upconversion is done using an up-converter and an RF oscillator signal (LO). This step produces an upconverted broadband signal at the RF band which has all the signals multiplexed in one stream. For the implemented system, we used the LO-frequency of 855MHz due to the challenges posed by the limited availability of narrow-band bandpass filters for high frequencies.

5) Analog signal multiplication: Multiplication of codes with RF-signal can only be carried out by using an analog multiplier. An analog multiplier produces the result which represents the multiplication of two analog signals. Mixers in a particular configuration can also be used as analog multipliers. The analog mixer form mini-circuits 15542 ZFM-5X 0-0148 model, with a response bandwidth of 1MHz-1500MHz was used for multiplication of the analog signals. This mixer covers the current system's LO frequency and the up-converted signal bandwidth. Thus, making it an ideal component for this task.

6) Splitting: Splitting the RF-upconverted signal into its identical copies is essential to our set-up. Split signal copies enable multiplication of the RF-signal with different CDM-codes in parallel. Thus allowing us to recover parallel and synchronised decoded signals. These signals should be in sync for the beamforming application. We used Mini-Circuit 4-way power-splitter ZN4PD1-50-S+ which supports a bandwidth of 500-5000MHz, to implement this part of the system.

7) RF Decoding: RF signal is multiplied with the code signals which were used for encoding. This multiplication recovers the corresponding upconverted RF signal for the baseband signal. The code signals are digital signals from the FPGA pins synchronized with the analog RF signal. A DC-block filter must be used to block the DC component in the digital code signals. DC-block filter results in a bipolar signal which is suitable for an analog multiplier. An analog multiplier (mixer) is required to multiply the RF up-converted signal with code signals. To implement the decoding part, we used mini-circuits 15542 ZFM-5X 0-0148 mixer and multiplied the analog upconverted signal with the code signals.

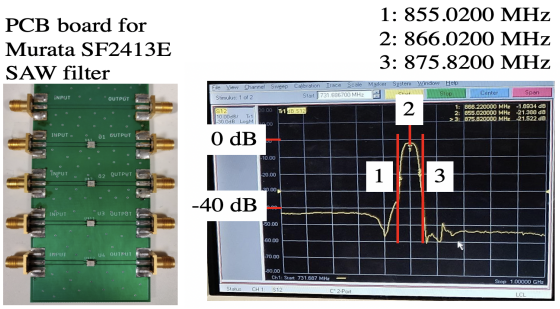

Fig. 5. a) Murata SF2413E Filter PCB b) S12 parameter of filter board.

8) Filtration: Proceeding RF decoding, the main signal should be at the center RF frequency with other signals around the spectrum separated by the coding rate between them. Hence, a narrow-band band-pass filter is vital to extract the required signal from the stream after multiplication. The bandwidth of RF-filter is based on factors such as the bandwidth of the signal multiplexed and the code rate that separates other components in the spectrum after we decode the signals. The required bandwidth of the filter is described as $Filter_{BW} = 2.xHz$, where x is the bandwidth/rate of the signal stream. Note, that the pass frequency of the filter should start at the RF upconversion frequency (LO). To fulfill these requirements we used a narrow-band band-pass SAW filter Murata SF2413E. The performance and specifications of the used filter are shown in figure 5.

9) Synchronization: To enable synchronization, a programmable delay line is used to set the right path delay for code signals. The firmware code sets the value of delay. Thus a user can set the value using a serial connection on a live system to achieve synchronization. The effect of synchronization depends upon the codes selected. If the codes used have different frequencies and are orthogonal, then the effect is observed on the output decoded signal's power, but phase information stays intact. Whereas, if the codes used have same frequency and are orthogonal, we observe the phase distortion along with change in power of the recovered signals which can severely affect the beamforming performance. For the CDM system to operate with full accuracy in reproducing the signal after demultiplexing, we are required to minimize the delay between the signal and the code paths. For optimal performance, the delay due to path difference should be $\Delta d_{path} < T_{code}$, where T_{code} is the time period of the code pulse ($code\_rate/2$).

III. Experimental Results

A. Experimental setup

We implemented all the necessary component connections as shown in figure 6. We used four sine wave signals , $\pi/4$ phase apart from each other instead of a complex beamforming algorithm and fed it as input to our CDM-based beamformer system. Simple sine wave signals allowed us to evaluate the effect of CDM-coding, conversion and decoding system on the phase and amplitude of the recovered signals. We implemented phase changing algorithm, CDM-encoder and code delay control parts onto the Xilinx Virtex-7 FPGA development board. Interfaced to the FMC connector of the FPGA board we used

Analog Digital's ADFMCDA-Q2 DAC board to convert the digital data stream to an analog output. This analog output is connected to mini-circuits 15542 ZFM-5X 0-0148 mixer to upconvert the signal generated to RF band. LO signal for RF-upconversion is generated using Agilent Vector signal generator. The upconverted signal passes through a Mini-Circuit 4-way power-splitter ZN4PD1-50-S+, which creates in-phase four copies of the upconverted RF-signal. This copy of the upconverted signal is multiplied with the code signal from the FPGA board using the mini-circuits 15542 ZFM-5X 0-0148 mixers. Followed by this step the signal is filtered using a narrow-band SAW band-pass filter Murata SF2413E to extract the decoded signal and eliminate the spectrum noise. The filtered signal is analyzed and sampled using the high-speed Digital signal analyzer at 80GSPS sampling speed.

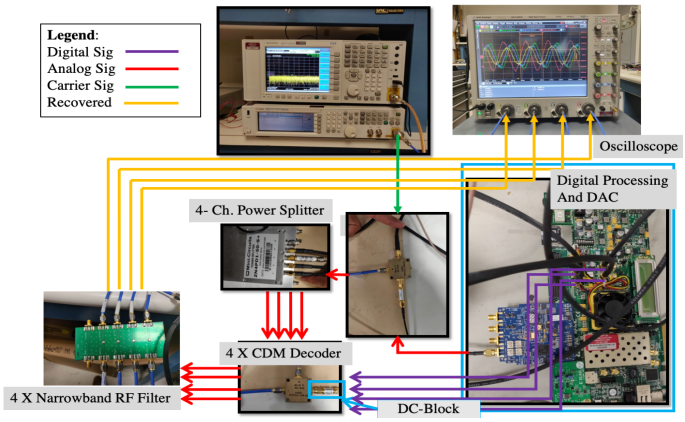

Fig. 6. Set-up of equipment used for the experiment.

B. Performance Analysis

To observe the performance of our system, we used MATLAB and the sampled data from the oscilloscope. This data was analyzed as though it was transmitted by ideal dipoles array(half wavelength spaced) to evaluate the resultant beam pattern and was compared to the ideal case.

1) Recovered Signals: Recovered signals are plotted in Figure 7. We can observe that the signals received are maintaining the relative phase and amplitude information also a necessary condition for beamforming. The power of the signals recovered after decoding is very faint. Hence, we can observe that there is noise present in the signals. This noise is the sampling noise and has a frequency of 79.99GHz(80GS/s) which is the sampling frequency for the oscilloscope in our case.

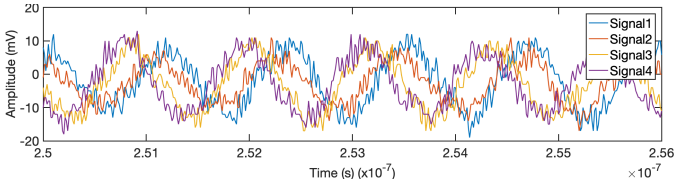

Fig. 7. Recovered signals at the oscilloscope.

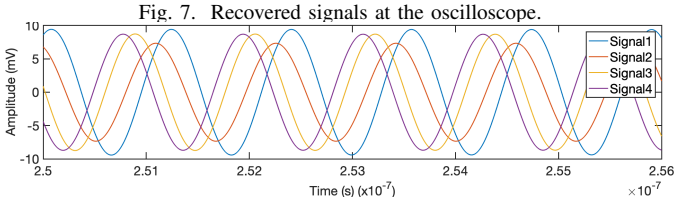

Fig. 8. Recovered signals after filtering out sampling noise.

2) Filtering out the sampling noise: The sampling noise is filtered out to eliminate any false patterns in the beamforming pattern. This is done using the MATLAB digital signal processing toolbox. The signals after eliminating the sampling noise are shown in figure 8. The slight phase distortion in signal 2 and 3 is due to sync issue as the codes used for these were of same frequency and orthogonal.

C. Beamforming with recovered signals in MATLAB

To mimic the case, we generated original signals (4 sine wave signals $\pi/4$ phase apart) in MATLAB simulation and fed them to ideal dipoles $\lambda/2$ apart to generate ideal results. Followed by that the recovered signals were fed to the same simulation antenna setup and its performance was benchmarked with the ideal case. The results of beamforming performance are shown in the figure 9.

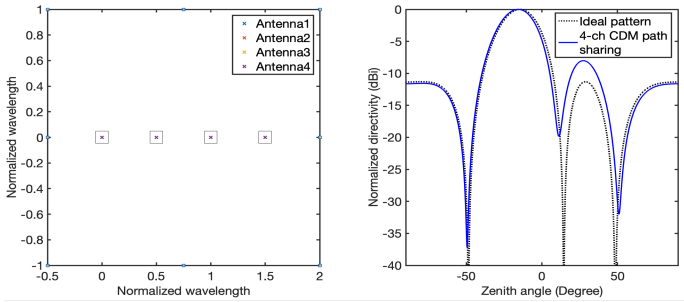

Fig. 9. Beamforming plots from recovered signals and ideal signals generated.

IV. CONCLUSIONS

In this paper, we successfully demonstrated the design of a low-cost CDM digital beam former transmitter, and validated it by making a system that can demonstrate beamforming using 4 antenna elements and uses only 1 DAC. This design and it's validation paves the way for wide application of the digital beamforming technology in wireless systems. The design is scalable to be used with more number of channels and with other RF frequencies. This new proposed system can reduce the system cost, enable energy savings and allow compact size beamforming systems. Thus, setting the direction for future wireless system designs.

REFERENCES

[1] R. B. Ertel, P. Cardieri, K. W. Sowerby, T. S. Rappaport, and J. H. Reed, "Overview of spatial channel models for antenna array communication systems," *IEEE personal communications*, vol. 5, no. 1, pp. 10–22, 1998.

[2] L. C. Godara, "Application of antenna arrays to mobile communications. ii. beam-forming and direction-of-arrival considerations," *Proceedings of the IEEE*, vol. 85, no. 8, pp. 1195–1245, 1997.

[3] C. A. Balanis, "Antenna theory: A review," *Proceedings of the IEEE*, vol. 80, no. 1, pp. 7–23, 1992.

[4] J. Litva and T. K. Lo, *Digital beamforming in wireless communications*. Artech House, Inc., 1996.

[5] E. A. Alwan, A. A. Akhiyat, W. Khalil, and J. L. Volakis, "Analytical and experimental evaluation of a novel wideband digital beamformer with on-site coding," *Journal of Electromagnetic Waves and Applications*, vol. 28, no. 12, pp. 1401–1429, 2014.

[6] D. Siafarikas, E. A. Alwan, and J. L. Volakis, "Processing gain using cdma in ultra-wideband multi-channel digital beam-formers," in *Antennas and Propagation & USNC/URSI National Radio Science Meeting, 2017 IEEE International Symposium on*. IEEE, 2017, pp. 935–936.

[7] D. S. Goshi, Y. Wang, and T. Itoh, "A compact digital beamforming smile array for mobile communications," *IEEE transactions on Microwave Theory and Techniques*, vol. 52, no. 12, pp. 2732–2738, 2004.
[8] A. Jahanian, F. Tzeng, and P. Heydari, "Code-modulated path-sharing multi-antenna receivers: theory and analysis," *IEEE Transactions on Wireless Communications*, vol. 8, no. 5, 2009.