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VSC Based Active Synchronizer for Generators

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***Abstract*--Fast synchronization of generators and microgrids will be a critical technology in future power systems with high penetration of non-dispatchable power resources. Existing synchronization methods rely on generator controls and their performance is limited by the generator characteristics. Speed of microgrid synchronization is further limited by the communication link among generation units. These factors lead to a slow and sometimes faulty synchronization, predominantly because of the phase mismatch during interconnection. This paper frames the generator synchronization problem as a phase-locked loop (PLL) design problem and introduces a voltage-source converter (VSC) based synchronizer for implementing the PLL based active synchronization method. The VSC based synchronizer is connected at the point of common coupling and it relies only on local measurements for control. It ensures zero phase error during interconnection by taking the advantage of the fact that the phase is not regulated in the generator controls. Relation between the synchronizer rating, control design, and synchronization speed is developed using describing function analysis of frequency and phase control loop gains. The operation and performance of the VSC-based synchronizer is demonstrated using simulations of a 555 MVA, 24 kV synchronous generator.**

***Index Terms*--Synchronization, microgrid control, distributed generators, automatic synchronizer.**

I. Introduction

With the increasing penetration of non-dispatchable renewable energy resources in power systems, it is becoming important to be able to quickly dispatch generation units whenever demanded by the load dispatch centers. Before a generator can be connected to a power system, the frequency, phase, and amplitude of the voltages at its bus need to be matched with those of the power system at the point of common coupling (PCC) [1, 2]. Hence, fast synchronization is critical to reduce the interconnection time.

Synchronization of conventional generators is achieved through generator controls, including the frequency and voltage control [2-4]. The generator controls are structured into hierarchical levels including primary, secondary, and tertiary level controls. Secondary control is implemented at a central location and it communicates references to the primary control of geographically distributed generators. Generator synchronization is achieved locally in the primary control [2-4]. Fast synchronization, however, is difficult using the existing method as the primary control bandwidth is limited by the generator characteristics, e.g. mechanical inertia. Moreover, the phase synchronization is usually achieved passively by a frequency offset between the generator and power system [2, 3]. This makes the interconnection time highly variable and dependent on the initial phase error and frequency offset. Higher frequency offset can reduce the phase-locking time [2], but results in a larger disturbance during interconnection. Active phase synchronization has been proposed in [5] by adding a term depending on the phase error to the generator frequency control loop. However, it is necessary to design the phase control much slower than the frequency control to avoid unstable interaction between them. The frequency control of generators is already very slow and the above requirement results in even slower phase synchronization. Hence, active phase synchronization based on the generator controls gives little advantage over the passive phase synchronization approach. Phase synchronization is more critical than the voltage and frequency synchronization for reducing the inrush currents [1]. Unreliable phase synchronization and indeterminate breaker operation time may lead to an out-of-phase synchronization and generator damage [6].

Synchronization of microgrids is achieved in similar manner as synchronous generators and suffers the same problems. Additionally, as the synchronization parameters at the PCC of a microgrid depend on several distributed generators, the synchronization function is implemented in the secondary control [7, 8]. Hence, the microgrid synchronization speed is further limited by the communication system of the secondary control [9-12]. Same as synchronous generators, the phase synchronization in microgrids is achieved either passively [13] or by introducing a correction term, depending on the phase error, in the microgrid frequency control loop [14-17]. However, phase being an ac variable unlike the voltage and frequency magnitudes, phase synchronization performance is particularly limited by the communication speed when achieved by distributed generator controls.

The above discussion highlights two problems: 1) control design framework to avoid interaction between the frequency and phase synchronization of generators and microgrids is not studied (this is important because of the discontinuous nature of the phase error); and 2) achieving fast synchronization, particularly the phase synchronization, is challenging when implemented through generator controls. This paper addresses the above problems by framing the generator and microgrid synchronization problem as a phase-locked loop (PLL) design problem and introducing a VSC-based synchronizer at the PCC of the generator or microgrid to be synchronized. The

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proposed VSC-based synchronizer relies only on local measurements and actively regulates the phase angle of the incoming generator or microgrid. Hence, zero phase error can be maintained during the breaker operation. Control system of the synchronizer is implemented using a phase-locked-loop (PLL) structure [18, 19], in which the generator or microgrid to be synchronized is treated as an oscillator. The PLL structure provides a design framework for avoiding interaction between the frequency and phase control loops. Relation between the synchronizer rating, control design, and synchronization speed is presented using describing function analysis. It is shown that the proposed synchronizer can reduce the synchronization time by an order of magnitude, even when it is rated at less than one percent of the generator rating. Operation and design principles of the VSC-based synchronizer are demonstrated using detailed simulations of a 555 MVA, 24 kV synchronous generator.

The rest of the paper is organized as follows: Section II reviews the existing synchronization method using generator controls. Section III frames the generator synchronization problem as a PLL design problem and introduces a VSC-based synchronizer for achieving fast synchronization. Control design, sizing, and performance evaluation of the synchronizer are presented in Section IV. Section V concludes this paper.

II. Synchronization using Generator Controls

Fig. 1 illustrates existing method of synchronization using generator controls [3-8]. In this method, the frequency and amplitude of the generator output voltages are slowly brought to the grid frequency and voltage levels using the primary control of the generator. When the synchronization process is initiated, the error between the generator and grid frequencies $\Delta\omega$ is processed by a synchronization controller, as shown in Fig. 1c). Based on the controller output, the primary control modulates the mechanical input power P_m to the generator to eliminate the frequency error. The voltage amplitude is similarly synchronized by modulating the input voltage to the field windings of the generator (E_{fd}). The phase synchronization is achieved by a frequency offset between the generator and grid frequencies. Because of the frequency difference, the phase error keeps changing with time. Once the frequency, phase, and voltage errors come within stipulated limits, usually referred as synchronization window [2], the generator breaker is closed.

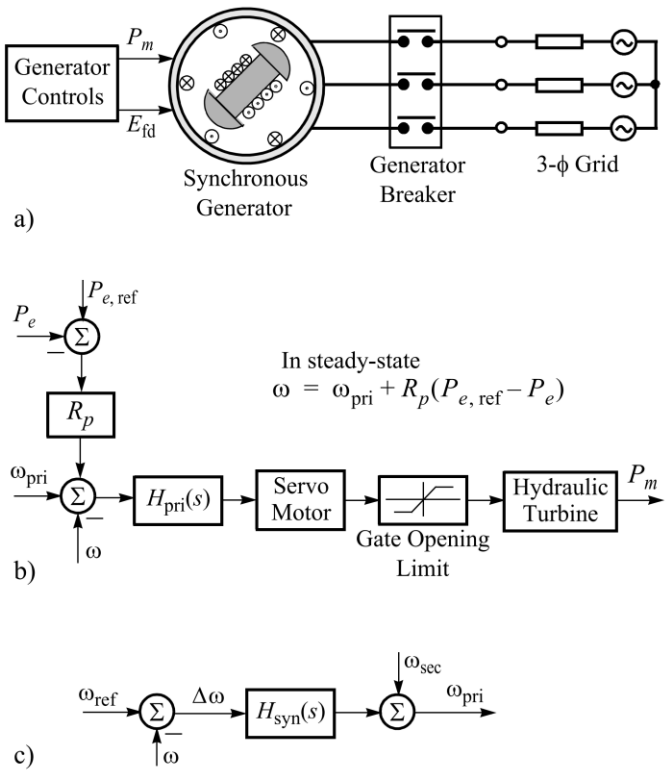

Fig. 1. Synchronization using generator controls. a) generator to be connected with the grid, b) primary control and c) synchronization control of the generator.

This paper focusses on the frequency and phase synchronization and assumes that the voltage levels are always synchronized because of the following reasons: i) voltage control can be easily achieved by field current (generators) or reactive power (microgrids) control, ii) voltage control does not involve conflict as in the frequency and phase control, and iii) the voltage matching requirement is much less important for a smooth synchronization than the frequency and phase matching requirements [1, 2].

The above discussed synchronization process is demonstrated in Fig. 2 for a 555 MVA, 24 kV generator. Generator parameters are taken from example 3.1 and 3.2 in [20]. Major parameters are also provided in the appendix. Fig. 2a) and b) respectively show the frequency and phase synchronization. Fig. 2c) shows inrush currents after closing of the generator breaker. It is to be noted that because of the synchronization process before the breaker operation, the peak inrush current is much lower than the generator peak rating current of 18.67 kA. The generator breaker is closed when the frequency and phase errors are within the following limits [2]:

$$\Delta f \le 0.05 \text{ Hz}, \Delta\theta \le 0.5^{\text{o}} \quad (1)$$

Because of the slow bandwidth of the synchronization control loop with the time constant of 120s, the synchronization process takes around 300s.

Microgrid synchronization is achieved in a similar manner, except for the fact that the synchronization controller is implemented at a remote location in the secondary control.

III. VSC-Based Active Synchronizer

A. PLL Based Active Synchronization

Generator or microgrid and main power system can be considered as two self-sustained oscillators that need to be synchronized. Hence, methods for the synchronization of oscillators [21] can be applied for generator synchronization. With generator treated as an oscillator, its synchronization problem can be formulated as a phase-locked loop (PLL) design problem. The PLL structure allows simultaneous control of the frequency and phase without conflict.

A PLL consists of three components: phase detector, loop filter, and internal oscillator [18], as shown in Fig. 3. Phase

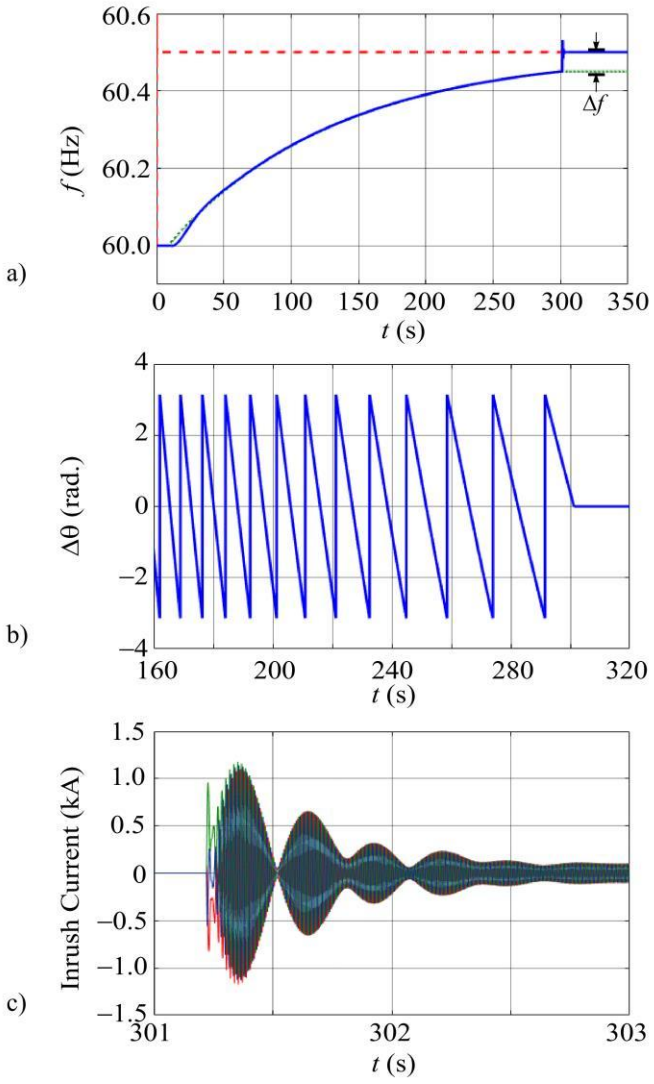

Fig. 2. Synchronization using generator controls. a) frequency in Hz; solid line is the generator frequency, dashed line is the power system frequency, and dotted line is the primary control frequency reference, $\omega_{pri}/2\pi$, b) phase error $\Delta\theta$, and c) inrush currents during the generator breaker operation.

detector estimates error between the phases of an external signal and internal oscillator. The phase detector output is passed through a loop filter to remove high frequency components. The loop filter output serves as frequency reference for an internal oscillator, which is usually implemented using an analog or digital circuit. For a properly designed PLL, the phase error between the external signal and internal oscillator goes to zero after any disturbance. For generator or microgrid synchronization using the PLL structure, an additional frequency control mechanism is required to track the frequency reference from the loop filter. The generator frequency can be controlled by modulating either its input power using the generator controls or its output power using a power converter at the generator terminals. Microgrid frequency can be similarly controlled for implementing the PLL based synchronization. Any PLL structure [18, 19] and frequency control mechanism can be used to implement the PLL based active synchronization method.

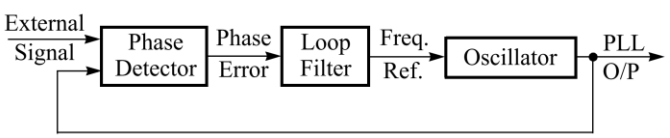

Fig. 3. PLL structure.

B. VSC-based Synchronizer

The PLL based synchronization is realized using a two-level voltage source converter (VSC) based synchronizer. The VSC-based synchronizer is connected at the PCC of a generator or microgrid to be synchronized. Synchronizer operation and design are demonstrated for a synchronous generator. Synchronizer will have similar performance for microgrids with high penetration of synchronous machine based generators. Possible issues that may arise in microgrids with high penetration of converter based generators are discussed in the following section.

Fig. 4 shows the VSC-based synchronizer connected at the PCC of a generator to be synchronizer. The VSC is supplied by a dc voltage source of magnitude V_{dc}. The dc source can be realized using batteries or by a power converter interfacing with the main power system, resulting in a back-to-back converter configuration. Back-to-back converter configuration at the front-end of a synchronous machine has been used in applications requiring variable-speed operation of the generator, such as pumped-hydro energy storage [22] and type-IV wind turbines [18]. These applications, however, require full-scale power converters as the power is always processed through the converters. The VSC-based synchronizer, on the other hand, is operated only during the synchronization process. It will also be shown that the synchronizer rating is required only to be a small fraction of the generator rating.

The synchronizer regulates the frequency and phase at the PCC by controlling the active power output from the VSC. Synchronous reference frame (SRF) based three-phase PLLs [18], shown in Fig. 4c), are used for obtaining the phase angle, frequency, and amplitude of three-phase voltages. Hence, two PLLs are used, one each for the generator and power system. Both PLLs are designed with 30 Hz bandwidth. They implement the phase detector function by obtaining the phase error:

$$\Delta\theta = \theta_{ref} - \theta \tag{2}$$

where θ_{ref} and θ are respectively the phase angles of the power system and generator output voltages. Fig. 4b) shows cascade implementation of the frequency and phase control loops to implement the PLL structure shown in Fig. 3. The phase error $\Delta\theta$ is passed through a phase-control compensator $H_\theta(s)$, which acts as the loop filter of Fig. 3. As shown in Fig. 4b), $H_\theta(s)$ gives frequency reference for the oscillator, which in this case is the generator to be synchronized. To eliminate initial transients, the power system frequency ω_{ref} is added to the output of $H_\theta(s)$.

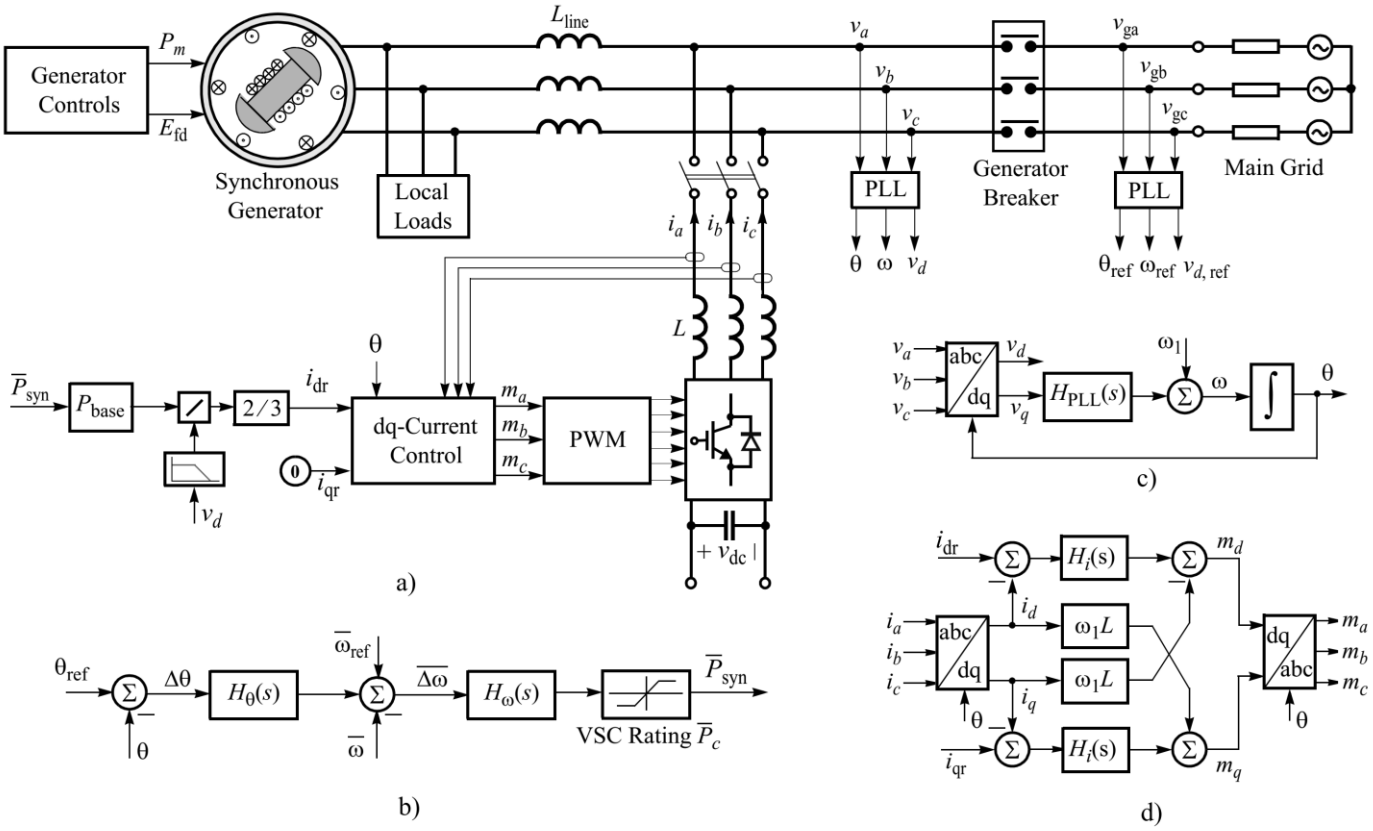

Fig. 4. Active synchronization of generator. a) Synchronous generator with VSC-based synchronizer, b) frequency and phase synchronization control implementation, c) phase-locked loop (PLL), and d) VSC ac current control in the dq-domain.

Based on the frequency error $\Delta\overline{\omega}$, the frequency-control compensator $H_\omega(s)$ generates reference for the active power output $\overline{P}_{syn}$ of the VSC-based synchronizer. Finite synchronizer rating is represented by a saturation block at the output of $H_\omega(s)$. Active power output from the VSC is regulated by controlling the output current i_{abc} using dq-domain current control shown in Fig. 4d). It is to be noted that overline indicates per unit (p.u.) values. Unless stated otherwise, parameters from appendix are used for the synchronizer.

C. Operation in the Absence of Generator Controls

To avoid conflict between the generator controls and the VSC based synchronizer, the generator controls are disabled during the synchronization process. This is realized by freezing P_m and E_{fd} (ref. Fig. 4) during the synchronization process. Fig. 5 demonstrates the operation of the VSC-based synchronizer. After initiating synchronization at 10s, frequency locking occurs at around 17s depending on the power supplied by the synchronizer. To distinctly demonstrate frequency and phase synchronization, the phase control is activated at 20s. Once the frequency and phase errors are reduced below the offsets defined in (1), the generator breaker is closed. Fig. 5c) shows power output from the VSC during the synchronization process. It is to be noted that the VSC rating is kept just one percent of the generator rating. The inrush currents in Fig. 5d) are smaller than those in Fig. 2c) because of the active phase synchronization.

D. Operation in the Presence of Generator Controls

If the VSC-based synchronizer is used for a microgrid or if the generator is located far from the PCC, it may not be possible to disable the generator controls during the synchronization process. Under such scenario, the generator controls may counteract the synchronizer action because of the mismatch in their operation speeds. For example, when the synchronizer tries to increase the generator frequency by injecting power at the PCC, as in Fig. 5a), the generator controls will try to maintain the frequency by reducing the power input P_m to the generator. Hence, after initial buildup in the frequency because of the synchronizer action, it will return to the trajectory followed when the synchronization is achieved only by generator controls. Nonetheless, difference between the speeds of the VSC-based synchronizer and generator controls can be leveraged to reduce the synchronization time.

Fig. 6 demonstrates synchronizer performance in the presence of the generator controls. Initially, the generator controls are allowed to execute synchronization, as in Fig. 2. When the frequency error is low enough, the VSC based synchronizer is activated to quickly synchronize the frequency and phase. If the converter based synchronizer is activated when the frequency error is too high, the generator controls will start acting before the synchronization is complete and will nullify the synchronizer action. Higher rating of the converter based synchronizer permits higher frequency error at which the synchronizer can be activated.

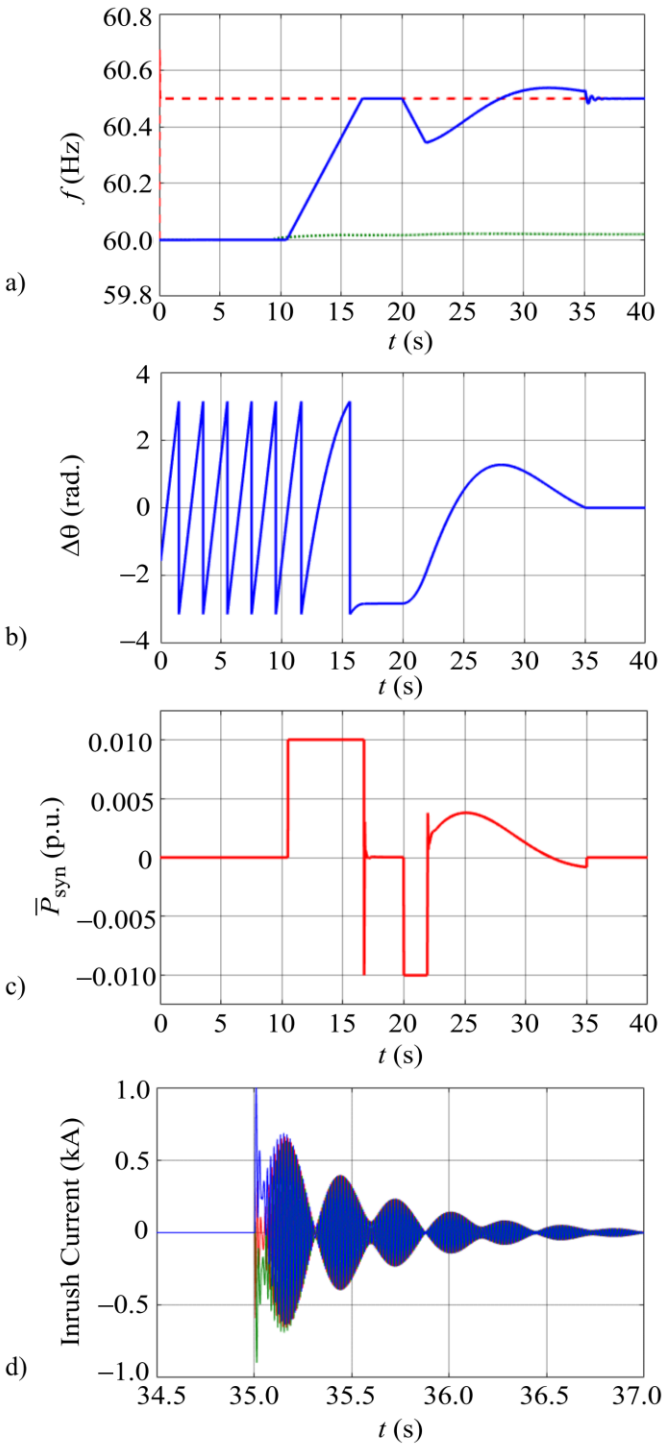

Fig. 5. Synchronization using VSC-based synchronizer. a) frequency in Hz; dashed line is the grid frequency and solid line is the generator frequency, b) phase error in radians, c) VSC power output, and d) inrush currents during the breaker operation. Generator controls are disabled during synchronization.

E. Operation during Grid Disturbance

It is important to evaluate the synchronizer performance in presence of grid disturbances such as harmonics, voltage sags, and phase jumps. Fig. 7 shows synchronization in the presence of 10% 7th harmonic and 5% 13th harmonic in grid voltages. The synchronizer operation is unaffected by the harmonics. This can be attributed to low bandwidths of the frequency and

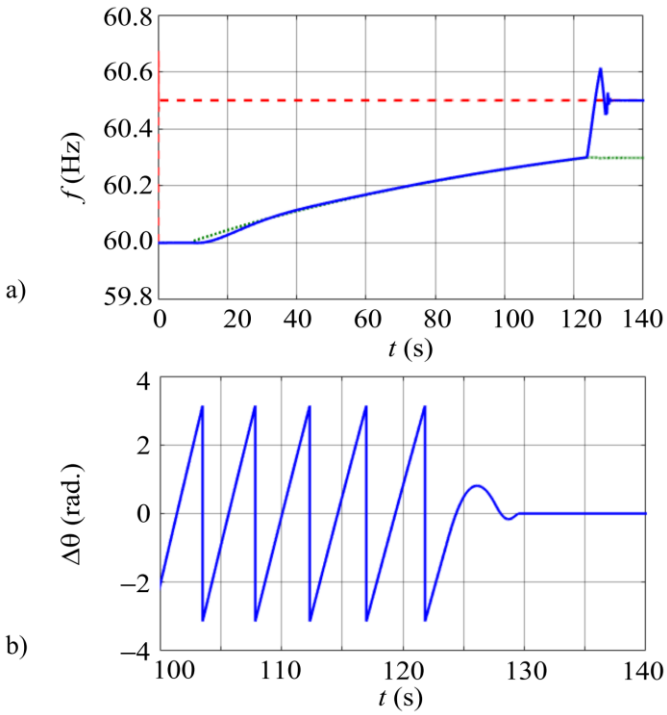

Fig. 6. Synchronization using VSC-based synchronizer in the presence of generator controls. a) frequency in Hz; dashed line is the grid frequency and solid line is the generator frequency, b) phase error in radians. VSC-based synchronizer is activated when the frequency error becomes less than 0.2 Hz.

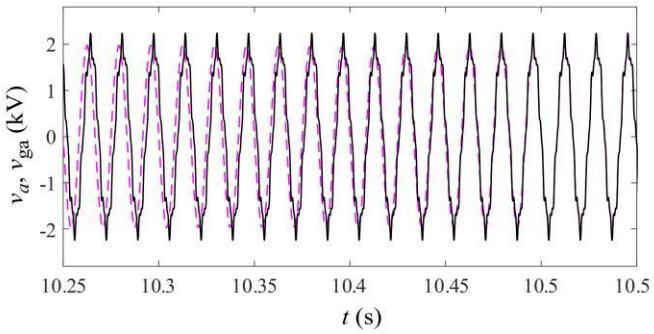

Fig. 7. Synchronization in the presence of harmonics in grid voltages (10% 7th harmonic and 5% 13th harmonic). Solid line: grid voltage and dashed line: generator voltage.

phase control loops of the synchronizer. The grid disturbances enter the synchronizer control system through SRF-PLLs used to implement the phase detector function in Fig. 4. Hence, effects of grid disturbances on the synchronizer performance can be mitigated by an appropriate PLL design [18].

IV. Control Design and Sizing

A. Frequency Control Design

Bandwidth of the VSC current control in Fig. 4 is limited by the converter switching frequency. In the simulation examples, the switching frequency is kept 2 kHz and the current control compensator $H_i(s)$ is designed for 200 Hz bandwidth.

For designing the frequency compensator $H_\omega(s)$, we need to obtain the frequency control loop-gain:

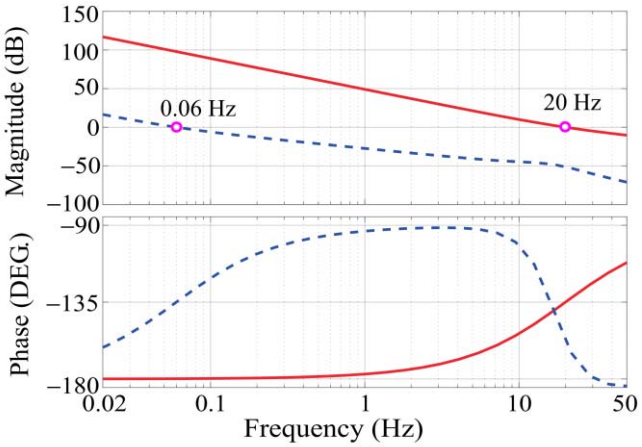

Fig. 8. Bode plot of frequency and phase control loop-gains for an ideal VSC-based synchronizer (infinite rating). Solid lines: frequency control loop-gain; dashed lines: phase control loop-gain.

$$L_{\omega}(s) = H_{\omega}(s) \cdot \frac{\Omega(s)}{\bar{P}_{\text{syn}}(s)} \tag{3}$$

where the second term on the right-hand side represents transfer function from the synchronizer power reference $\bar{P}_{\text{syn}}$ to generator frequency in rad/s. As the frequency control bandwidth is designed much lower than the VSC current control bandwidth, the active power injected by the VSC-based synchronizer can be considered equal to the reference $\bar{P}_{\text{syn}}$.

Generator frequency (speed) dynamics can be described as

$$\frac{d\bar{\omega}}{dt} = \frac{1}{2H}\left(\bar{P}_m - \bar{P}_e\right) \tag{4}$$

where $\bar{P}_m$ and $\bar{P}_e$ are respectively the mechanical power input and the electrical power output in p.u., and H is the inertia constant in seconds. Injection of power by synchronizer is equivalent to reducing the generator output power $\bar{P}_e$ by the same amount. Hence, the following relation holds in the small-signal sense as:

$$\bar{P}_{\text{syn}}(s) = -\bar{P}_e(s) \tag{5}$$

Depending on the generator controls, P_m will react to any change in the generator frequency ω. Hence, the loop-gain in (3) will also depend on the generator controls. If the generator controls are disabled during the synchronization process, P_m remains constant and the following relationship is obtained using (4) and (5):

$$\frac{\Omega(s)}{\bar{P}_{\text{syn}}(s)} = \frac{1}{2Hs} \tag{6}$$

Frequency compensator is designed to give bandwidth of 20 Hz. Response of $L_{\omega}(s)$ is shown in Fig. 8.

It is to be noted that the rate-of-change-of-frequency (ROCOF) during generator synchronization may be limited to avoid excessive torsional stresses. In microgrid synchronization, a high ROCOF may also trigger protection functions such as islanding detection [23] and under-frequency load-shedding (UFLS) relays [24]. ROCOF limits are not considered in this paper; however, they can be easily incorporated in the synchronizer controls.

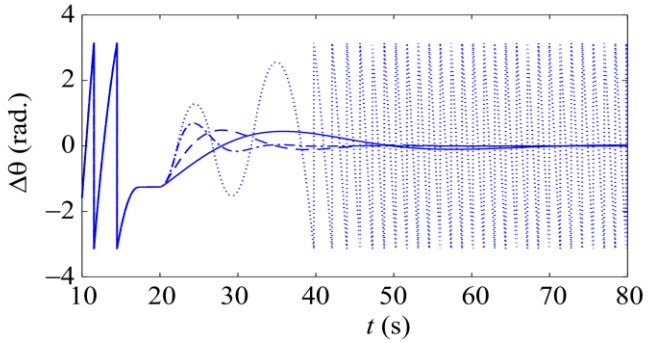

Fig. 9. Phase error response for different phase-control bandwidths demonstrating limitation on the bandwidth imposed by the synchronizer rating. Bandwidth: 0.03 Hz (solid lines), 0.06 Hz (dashed lines), 0.12 Hz (dashed-dotted lines), and 0.15 Hz (dotted lines).

B. Phase Control Design

For designing the phase compensator $H_{\theta}(s)$, the frequency control dynamics can be ignored if the phase control bandwidth is much lower than the frequency control bandwidth. Under this condition, the phase control loop-gain is

$$L_{\theta}(s) = H_{\theta}(s) \cdot \frac{\omega_1}{s} \tag{7}$$

where the integrator converts the frequency output from the frequency control loop to phase angle. Base frequency ω_1 converts the frequency control output from p.u. to absolute value.

With the frequency control bandwidth of 20 Hz, the phase control bandwidth can be easily designed to be around 2 Hz. However, simulated responses in Fig. 9 show that the phase control becomes unstable for bandwidths above 0.12 Hz. This is because of the finite rating of the converter based synchronizer, as explained in the following subsection. Hence, the phase control bandwidth is designed to be 0.06 Hz, as shown in Fig. 8.

C. Synchronizer Rating: Effects and Control Design

Cost considerations require that the VSC-based synchronizer rating is as small as possible. However, a finite synchronizer rating limits the maximum permissible bandwidth of the phase control loop. Rating of the synchronizer, denoted by $\bar{P}_c$, manifests as saturation, as shown in Fig. 4b). Conditional integration based anti-windup scheme is employed in the PI compensator $H_{\omega}(s)$ to avoid integration windup because of the saturation block. The anti-windup scheme stops integration whenever the output of $H_{\omega}(s)$ hits either of the saturation limits $\pm\bar{P}_c$ and the polarity of the compensator input $\Delta\bar{\omega}$ is the same as that of the violated limit [25].

For control design, the saturation block in Fig. 4b) can be

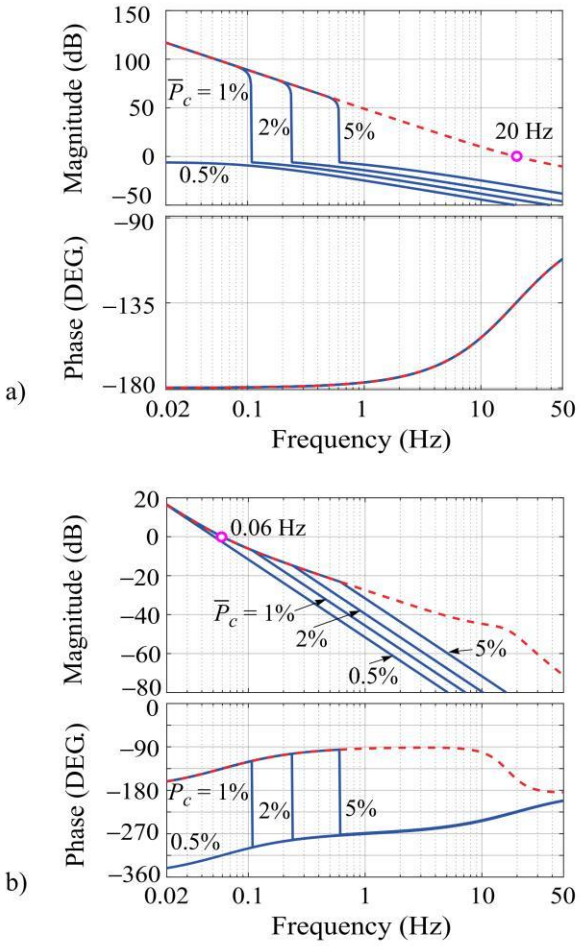

Fig. 10. Bode plot of a) frequency-control and b) phase-control loop gains. Solid lines show responses for different VSC-based synchronizer ratings, represented as the percentage of the generator rating. Dashed lines show response for the ideal synchronizer (infinite rating).

represented by its describing function [26]. Describing function of a nonlinearity is its large-signal gain from a single-sinusoidal input signal to the nonlinearity output component at the input frequency. Describing function of the saturation block in Fig. 4b) is [26]:

$$N(A)=\begin{cases}1 & \text{for } A\le \bar{P}_c \\ \dfrac{2}{\pi}\left[\sin^{-1}\left(\dfrac{\bar{P}_c}{A}\right)+\dfrac{\bar{P}_c}{A}\sqrt{1-\left(\dfrac{\bar{P}_c}{A}\right)^2}\right] & \text{for } A>\bar{P}_c\end{cases} \quad (8)$$

where A is the amplitude of the input signal to the saturation block. It is evident from (8) that the saturation block gain is unity whenever the output of $H_\omega(s)$ is less than $\bar{P}_c$. The gain starts decreasing as A increases beyond $\bar{P}_c$. This reduces the effective frequency control bandwidth. Consequently, it requires reduction in the phase control bandwidth to avoid interaction between the frequency and phase control loops.

Even after knowing the amplitude-dependent gain of the saturation block, it is not possible to obtain responses of the frequency and phase control loop-gains as the amplitude A is unknown. However, the worst-case amplitude A can be determined by noting that it is the same as the maximum possible value of A. We know that the maximum phase error, which is the input to $H_\theta(s)$, is π. Hence, A for the worst-case scenario can be obtained by solving the following nonlinear implicit equation:

$$\frac{A}{\pi}=\left|\frac{H_\theta(s)\cdot H_\omega(s)}{1+H_\omega(s)\cdot N(A)\cdot\dfrac{\bar{\Omega}(s)}{\bar{P}_{syn}(s)}}\right| \quad (9)$$

The right-hand-side of (9) represents absolute gain from Δθ to the output of $H_\omega(s)$ in Fig. 4.

We can obtain responses of the frequency and phase control loop gains for different synchronizer ratings by solving (9) at each frequency for A and using it in (8). Solid lines in Fig. 10a) and b) respectively compare the frequency and phase control loop gains, $L_\omega(s)$ and $L_\theta(s)$, for different synchronizer ratings. Synchronizer ratings in Fig. 10 are represented as percentage of the total generator rating. Fig. 11 validates the analytical response of the phase control loop gain, obtained using (6), (8), and (9), against point-by-point simulations for the synchronizer of rating of 5%.

As the frequency control can easily track slow varying references without the error Δω becoming too large to saturate the synchronizer, the frequency and phase control loop-gain responses remain unaffected by the synchronizer rating at low frequencies. In other words, the saturation effect is manifested only above a certain critical frequency for a particular synchronizer rating (ref. Fig. 10a). It is evident from Fig. 10a) that as the VSC based synchronizer rating is reduced, the effective frequency control bandwidth also gets reduced. Detailed discussion on the effects of a saturation block on the loop-gain response can be found in [27].

To avoid instability observed in Fig. 9, the phase control bandwidth must be kept below the frequency at which the frequency control loop gain $L_\omega(s)$ starts decreasing at a fast rate because of the saturation effect. This frequency, denoted by ω_c, is approximately the same as the frequency at which amplitude A of the input signal to the saturation block becomes equal to the converter rating $\bar{P}_c$. Gain of the saturation block N(A) at this point is unity. Hence, (9) at ω_c can be written as

$$\frac{\bar{P}_c}{\pi}=\left|\frac{H_\theta(j\omega_c)\cdot H_\omega(j\omega_c)}{1+H_\omega(j\omega_c)\cdot\dfrac{1}{2H\cdot j\omega_c}}\right| \quad (10)$$

Rearranging the terms in (10), we get:

$$\frac{\bar{P}_c}{\pi}=\left|\left[\frac{H_\theta(j\omega_c)}{\dfrac{1}{2H\cdot j\omega_c}}\right]\cdot\left[\frac{H_\omega(j\omega_c)\cdot\dfrac{1}{2H\cdot j\omega_c}}{1+H_\omega(j\omega_c)\cdot\dfrac{1}{2H\cdot j\omega_c}}\right]\right| \quad (11)$$

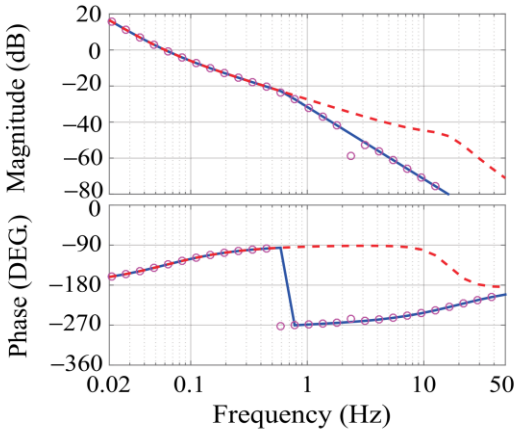

Fig. 11. Verification of the phase-control loop gain model. Solid lines show model response for synchronizer rating of 5%, circles show response obtained by point-by-point simulations, and dashed lines show response for the ideal synchronizer.

The term in the second set of brackets in (11) represents the frequency-control closed loop gain without considering the saturation effects. As ω_c is well below the designed frequency-control bandwidth, which is 20 Hz in the case studies presented here, the term in the second set of brackets is approximately equal to unity at ω_c. Hence, (11) simplifies to

$$\frac{\bar{P}_c}{\pi} = \left|2H \cdot j\omega_c \cdot H_\theta(j\omega_c)\right| \tag{12}$$

Assuming that $H_\theta(s)$ is realized by a PI compensator with the zero located at the phase control bandwidth ω_θ for achieving 45° phase margin, using (7), we get:

$$H_\theta(s) = \left(\frac{\omega_\theta^2}{\omega_1 \cdot \sqrt{2}}\right)\left[\left(1+\frac{s}{\omega_\theta}\right)/s\right] \tag{13}$$

Gain in (13) ensures that the magnitude of the phase control loop gain $L_\theta(s)$ is unity at ω_θ.

Using (12) and (13), the critical frequency ω_c can be determined as:

$$\omega_c = \sqrt{\frac{2}{\omega_\theta^2}\left(\frac{f_1 \cdot \bar{P}_c}{H}\right)^2 - \omega_\theta^2} \tag{14}$$

As phase of the loop-gain $L_\theta(s)$ decreases rapidly above ω_c (ref. Fig. 10b), the phase-control bandwidth ω_θ must be kept lower than the critical frequency ω_c to ensure sufficient phase margin. Using (14), this condition simplifies to:

$$\omega_\theta \text{ (in rad./s)} < \sqrt{\frac{f_1 \cdot \bar{P}_c}{H}} \tag{15}$$

It is interesting to note that the limit on the phase control bandwidth is directly related to the synchronizer rating, and it is independent of the frequency control bandwidth. This is expected, as the frequency control bandwidth is much higher than the frequency range at which the saturation is manifested (refer Fig. 10).

For H = 3.7s and $\bar{P}_c = 1\%$, using (15), the phase control bandwidth must be limited to 0.06 Hz. However, Fig. 10a) shows that the phase control bandwidth must be below 0.12 Hz for stability under the same conditions, which is also verified by simulations in Fig. 9. The discrepancy is because we assumed that the frequency control loop-gain starts decreasing rapidly right after the amplitude A hits the synchronizer rating $\bar{P}_c$. However, the loop-gain initially decreases only gradually before decreasing rapidly to a low value (refer Fig. 10a). Nonetheless, the condition in (15) can be used as a thumb rule, leading only to a slightly conservative design.

D. Synchronizer Performance and Rating

This subsection relates the time required for synchronization with the synchronizer rating. If the frequency difference between the generator and grid is Δf, the energy that needs to be exchanged with the generator to eliminate the frequency error is

$$E = \frac{1}{2}J \cdot \left[\left(2\pi \cdot f_{\text{ref}}\right)^2 - \left(2\pi \cdot f\right)^2\right] \approx 4\pi^2 J \cdot f_1 \cdot \Delta f \tag{16}$$

where J is generator mechanical inertia in kg·m^2. It is related with the inertia constant H as:

$$J = \frac{2H \cdot P_{\text{base}}}{\omega_1^2} \tag{17}$$

Time required for synchronizer of rating $\bar{P}_c$ to exchange energy E from (16) is given by

$$T_\omega = \frac{E}{\bar{P}_c \times P_{\text{base}}} \tag{18}$$

Time required for phase locking depends on the phase control bandwidth ω_θ. The phase-control loop forms a second-order system with the damping ratio ξ of 0.42 for the designed phase-margin of 45°. Moreover, its natural frequency is approximately the same as the bandwidth ω_θ. Hence, the settling time of the phase-control loop is given by:

$$T_\theta \approx \frac{4}{\xi \cdot \omega_\theta} > \frac{4}{\xi}\sqrt{\frac{H}{f_1 \cdot \bar{P}_c}} \tag{19}$$

Sum of the frequency and phase locking times from (18) and (19) gives the total synchronization time. It is evident that a lower rating of the synchronizer increases the time required for the synchronization process. Hence, there is a trade-off between the synchronizer rating and speed of the synchronization process.

The PLL structure avoids unstable interaction between the frequency and phase control loops. It is not necessary to achieve the frequency and phase locking sequentially as required in the existing methods [12]. Simultaneous frequency and phase synchronization results in total synchronization time to be lower than that predicted by (18) and (19). For Δf of 0.5 Hz and parameters from Appendix, the frequency and phase locking times from (18) and (19) are respectively 6.16s and

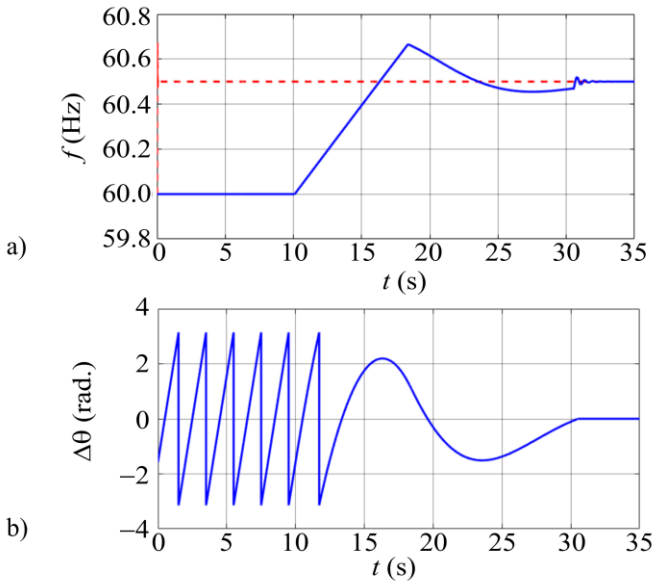

Fig. 12. Simultaneous operation of the frequency and phase control loops. Synchronization is achieved in 22s.

23.65s, predicting the total synchronization time of around 30s. Fig. 12 shows that the synchronization is achieved in 22s after the frequency and phase control loops are activated together at t = 10s.

E. Microgrid Synchronization

Fundamental to the operation of the VSC-based synchronizer is that the frequency at the PCC of the generator or microgrid to be synchronized is sensitive to the active power output of the synchronizer. This is given for a synchronous generator and the sensitivity is captured in (4). Such sensitivity is also present in microgrids with high penetration of synchronous machine based distributed generators. In such scenario, the transfer function from the synchronizer power reference $\overline{P}_{\text{syn}}$ to frequency ω at the PCC depends on the aggregated inertia in the microgrid. For microgrids with high penetration of converter based generators, however, the sensitivity of frequency towards active power flow is required to be emulated by controls. Most converter based microgrids use droop control for power sharing and the microgrid frequency is dependent on the active power flow. It is important to obtain the frequency response of the transfer function from $\overline{P}_{\text{syn}}$ to ω using measurements or modeling for designing the VSC-based synchronizer controls for such microgrids.

Additional dynamic present in microgrids is the line impedances between the distributed generators and between the microgrid and synchronizer. The frequency and phase synchronization dynamics are much slower than the electromagnetic dynamics introduced by transmission lines. Hence, they can be ignored in the synchronizer design. It is verified that even for a large variation in the transmission line inductance L_{line} between the generator and PCC in Fig. 4, the phase and frequency response during synchronization remains unaffected. The variation of the transmission line inductance considered in simulations is given in Table I; the maximum value of L_{line} corresponds to grid short-circuit ratio of as low as 2.5.

TABLE I GENERATOR PARAMETERS

Parameter	Value
Rating, P_{base}	550 MVA
Rated output voltage (rms), $V_{l\text{-}l}$	24 kV
Nominal frequency, f_1	60 Hz
Stator resistance, R_s	3.1 mΩ
Stator leakage inductance, L_l	0.413 mH
d-axis magnetizing inductance, L_{md}	4.569 mH
q-axis magnetizing inductance, L_{mq}	4.432 mH
Field winding resistance, R_f	0.0715 Ω
Field winding self inductance, L_{ffd}	576.92 mH
Inertia constant, H	3.7 s
Number of poles	2
Transmission line inductance, L_{line}	0 to 1.1 mH
Synchronization compensator, $H_{\text{syn}}(s)$	0.01 + 0.008/s

V. CONCLUSION

The existing methods of synchronization of generators and microgrids with the main power system rely on generator controls and the phase synchronization is usually achieved in a passive manner. This results in slow synchronization and long interconnection time. It may also lead to a faulty synchronization, as zero phase error cannot be ensured during the generator breaker operation. Another problem is the lack of design framework to avoid interaction between the frequency and phase synchronization, when the latter is achieved in an active manner. To address these problems, this paper framed the generator and microgrid synchronization problem as a PLL design problem. A VSC-based active synchronizer is introduced to implement the PLL based synchronization method. Using simulations of a synchronous generator and nonlinear describing function analysis, it is shown that the active synchronizer can reduce the synchronization time by an order of magnitude, even when it is rated less than one percent of the generator rating.

APPENDIX

Parameters from Table I and II are used respectively for the synchronous generator and the VSC-based synchronizer.

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TABLE II VSC-BASED SYNCHRONIZER PARAMETERS

Parameter	Value
VSC rating, $\overline{P}_c$	0.01 p.u. (5.5 MVA)
Rated output voltage (rms), $V_{l\text{-}l}$	24 kV
DC-bus Voltage, V_{dc}	48 kV
Phase reactor inductance, L_{ph}	45.0 mH
Phase reactor resistance, R_{ph}	2.3 Ω
Current control compensator, $H_i(s)$	$(2/V_{\text{dc}})\cdot(40 + 50\text{x}10^4/s)$
Decoupling gain, k_d	$(2/V_{\text{dc}})\cdot 2\pi f_1 L_{\text{ph}}$
Frequency control compensator, $H_\omega(s)$	$657.5 + 8.26\text{x}10^4/s$
Phase control bandwidth, ω_θ	$2\pi\cdot 0.06$ rad/s
Phase control compensator, $H_\theta(s)$	$(7.07 + 2.66/s)\text{x}10^{-4}$
Switching frequency, f_{sw}	2 kHz

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